

(ENGLISH TRANSLATION)

FIRST OFFICE ACTION

Date of Receipt: January 16, 2003

1. APPLICATION NO.: 91103681
2. TITLE: Mode switching method for PLL circuit and mode control circuit for PLL circuit
3. APPLICANT: Fujitsu Limited
ADDRESS: japan
4. PATENT ATTORNEY: Patrick I. C. Yun/William W. L. Chen
5. FILING DATE: February 27, 2002
6. PRIORITY DATA: Japanese application serial no. 2001-089880 filed 2001/03/27
7. CONTENTS OF ACTION:

Subject

The invention in this application shall not be granted an Invention Patent on the basis of Article 20.2 of the Patent Law.

Reasons

1. The invention in this application entitled, "Mode switching method for PLL circuit and mode control circuit for PLL circuit," relates to a switching and control method for a PLL circuit having two modes (*i.e.*, a high speed mode and a normal mode).
2. This invention is directed to a phase comparator for comparing the phase of a reference frequency-divided signal with the phase of a comparison frequency-divided signal and a charge pump for generating a current according to the output signal from the phase comparator. Current is generated in accordance with the charge pump and the current generates VCO and then, in accordance with the frequency of the VCO, the desired frequency of the first mode and the second mode is locked. It is noted that R.O.C. patent publication no. 387085 published April 11, 2000 (see attachment) entitled, "Read Channel IC for Dual Phase-Lock-Loop (PLL) Solution," discloses switching, through a phase detector, a charge pump and a VCO, the signal of the frequency divider to another charge pump and PLL, and utilizing the VCO in PLL which provides reference frequency and the comparator for switching to idle mode or other modes. Both inventions control the charge pump by division of the reference frequency and then detecting the phase with the phase comparator, which in turn affect the VCO to output different frequencies for switching to different modes. Therefore, the two inventions have the same technical principle. This invention differs only in that there is an additional prescaler after the VCO for feedback, whereas in the cited reference, the comparator takes the feedback and connects to the charge pump. Such change in the feedback does not involve inventive step.
3. In conclusion, this invention utilizes technology or knowledge in existence prior to its filing and can be easily achieved by one skilled in the art. This invention cannot be deemed to satisfy the requirements of an Invention Patent.

In view of the aforesaid, this invention is not in agreement with the provision in Article 20.2 of the Patent Law and accordingly shall not be granted a patent.

Sealed By
Lian-Sheng Tsai
Director

NOTE: If dissatisfied with this Office Action, the Applicant may file a request for reexamination along with a Response within thirty (30) days of the day following the date of receipt of this Office Action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-5 and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamanoi et al (U.S Patent No. 6,067,335 cited in PTOL 1449).

These claims are met by the circuitry and operation as disclosed relative to Figs 5A-5D, 6A-6B. These circuits disclose switching through a phase detector, a charge pump and a VCO, and controlling the charge pump by division of the reference frequency and then detecting the phase with the phase comparator, which in turn affect the VCO to output different frequencies for switching to different modes. First mode and second mode read on idle mode and read mode, switching the mode of the PLL circuit from the first mode to the second mode or the second mode to the first mode when the high impedance state is detected (during idle mode, 406-407 achieve lock using the output of the time base generator before switching over to read mode). The limitation "delay circuit" recited in claim 17 is inherent seen in col. 7, line 48. Element "LOOP FILTER 2" reads on "a low-pass filter" as recited in claim 18.

Allowable Subject Matter

Claims 2 and 6-16 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.